PATENT APPLICATION
DOCKET NO.: 200300032-2

REMARKS

Claims 1-16 are presented for examination, of which claims 1, 10, and 13 are in independent form. Claims 1, 10 and 13 have been amended by way of the present Response. Support for the amendments may be found in the present patent application in respect of FIG. 2 and associated description at Paragraphs [0018]-[0025], *inter alia*.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

Claims 1, 3-7, 10, 13, and 14 are rejected in the pending Office Action under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2004/0004975 to Shin et al. (hereinafter the *Shin* reference), in view of U.S. Patent Publication No. 2001/0040908 to Locker et al. (hereinafter the *Locker* reference) and U.S. Patent No 6,874,063 to Arimilli et al. (hereinafter the *Arimilli* reference).

Additionally, claims 2, 8, 9, 11, 12, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin* in view of *Locker*, *Arimilli* and U.S. Patent Publication No.

2004/0024946 to Naumann et al. (hereinafter the *Naumann* reference).

In connection with these rejections, the Examiner has commented as follows with respect to the base claims 1, 10, and 13:

> Consider **claims 1, 10, 13** Shin et al. clearly disclose and show a system for effectuating the transfer of data blocks including a header block (fig. 4 (410), fig. 5 (500 header); paragraph 9 (large header)) across a clock boundary (asynchronous clock boundary) between a first clock domain (paragraph 9 (transmitter's clock domain)) and a second clock domain (paragraph 9 (receiving device's local clock frequency)), wherein said first clock domain is operable with a first clock signal (paragraph 9 (transmitter's clock domain)) and said second clock domain is operable with a second clock signal (paragraph 9 (receiving device's local clock frequency)), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M>1 (paragraph 73 (transmitter's frequency is faster than the receiver's (an overrun condition))), comprising: a first circuit portion (fig. 2 (201 transmitter; fig. 3)) for providing said data blocks including said header block to a second circuit portion (fig. 2 (202 receiver; fig. 3)); control logic associated with said second circuit portion for processing said header block (fig.3; paragraphs 3 and 83 (control the transmission and reception of the symbols)).
>
> However, Shin et al. do not specifically disclose the sending of hint signal.

In the same field of endeavor, Locker et al. clearly shows the sending of hint signal (paragraph 28 (B sends the hint signal to A)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate the hint signal, as taught by Locker et al., so that appropriate element would be selected.

However, Shin et al., as modified by Locker, do not specifically disclose the ordering of data transfer.

In the same field of endeavor, Arimilli et al. clearly shows the ordering of data transfer (abstract (order bit for transmitting data in that order)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate hint signal, as taught by Locker et al., and ordering fr data transfer, as taught by Arimilli, so that data transfer between two clock domains is done efficiently. However, Shin et al., as modified by Locke, do not specifically disclose the ordering of data transfer.

Applicant respectfully submits that the pending §103(a) rejections as set forth above have been overcome or otherwise rendered moot by way of the present amendment. As defined by base claim 1, an embodiment of the present disclosure is directed to a system for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein the first clock

domain is operable with a first clock signal and the second clock domain is operable with a second clock signal. The claimed embodiment comprises, *inter alia*, a first circuit portion, a second circuit portion and control logic that are disposed in the first clock domain and a third circuit portion and associated control block that are disposed in the second clock domain. The control logic generates, in response to the header block, a hint signal that gives advance notification of a possible data transfer operation, with the hint signal operable to be transferred via a synchronizer to the second clock domain. The control block operates responsive to the hint signal to generate data transfer control signals for controlling the third circuit portion.

As defined by base claim 10, an embodiment of the present disclosure is directed to a method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain. The method comprises, *inter alia*, processing a header block associated with data blocks that are to be sent from the first clock domain to the second clock domain via a synchronizer and generating a hint signal that gives advance notification of a

possible data transfer operation responsive to the header block. The hint signal is positioned at least one cycle prior to the location of the data blocks, with the processing and generating being performed in the first clock domain. The hint signal is transmitted to a control block in the second clock domain, thereby indicating that the data blocks may be sent to receive circuitry in the second clock domain and appropriate control signals are generated based on the hint signal in order to control output of the data blocks in a particular ordered grouping. Substantially similar features are also recited in base claim 13.

The Examiner has acknowledged that the *Shin* reference does not disclose the sending of a hint signal as claimed. Furthermore, *Shin* does not teach or suggest that the hint signal gives advance notification of a possible data transfer or that the hint signal can be transferred across the boundary between two clock domains having different clock rates. Applicant respectfully submits that the *Locker* and *Arimilli* references do not cure the aforementioned deficiencies of the *Shin* reference.

The *Locker* reference is directed to cross-coupled phase lock loop circuits that provide pseudo-synchronization between two

independent clock signals. See Abstract. *Locker* notes that the two clock signals are synchronized to each other and to a common system clock. The two clock signals are also required to remain in the same clock cycle.

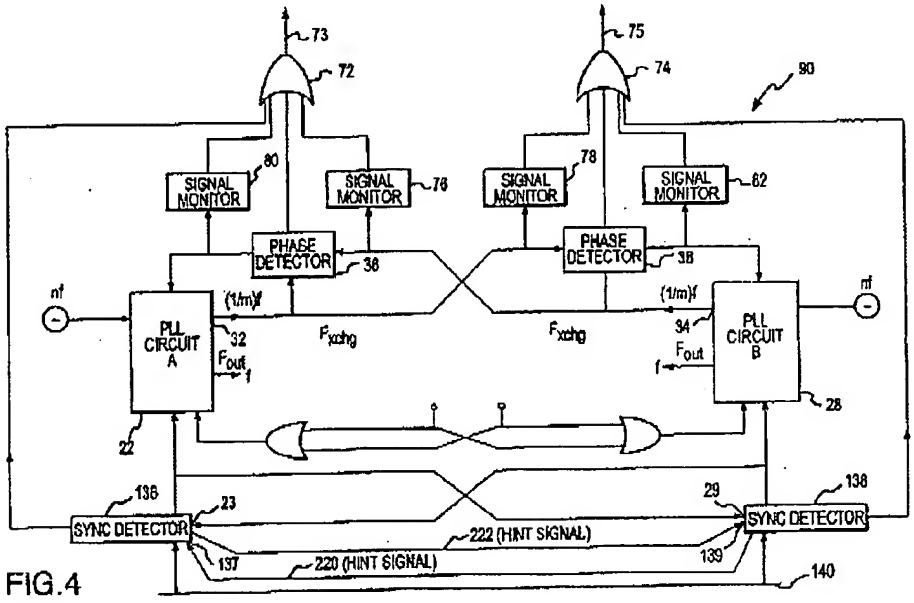

FIG.4

FIG. 4 of *Locker*, reproduced herein for convenience, discloses system 90, which maintains pseudo-synchronization between clock signal F_{out} of PLL circuit A and clock signal F_{out} of PLL circuit B. Phase detectors 36, 38 monitor the relationship between sampling signals F_{xchng} 32, 34 and, when one of these

signals lags behind the other, retards the phase of the leading clock signal as necessary so that the two output signals are brought back into approximate synchronization. See Paragraphs [0015], [0016] and [0024]. Clocks F_{out} A and F_{out} B are synchronized with the system clock using a sync signal from system sync bus 140. If the sync signal is detected near the boundary of two cycles, the skew between the two clocks may cause sync detector 137 to detect the sync signal as being in one clock cycle and sync detector 139 to detect the sync signal as being in another clock cycle. To maintain the pseudo-synchronization, sync detectors 137, 139 send hint signals 220, 222 to each other to ensure that both clocks will synchronize together. See Paragraphs [0024]-[0027].

Hint signals 220, 222 of *Locker* are not used in respect of a possible data transfer operation. Nor are hint signals 220, 222 sent across a clock boundary between two clocks having different frequencies (i.e., the first and second clock signals recited in the claims have a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1). Accordingly, *Locker* does not make up for the deficiencies of the *Shin* reference.

The *Arimilli* reference is directed to a method for informing a processor of a selected order of transmission of data to the processor. The preference order is provided by the processor as a selected order bit and can be compared to the preference order provided by other entities, with one preference order being selected and the data retrieved in that order. See Abstract. *Arimilli* does not use hint signals and does not meet the limitations of generating, in response to the header block, a hint signal that gives advance notification of a data transfer operation, the hint signal being operable to be transferred via a synchronizer. Accordingly, *Arimilli* does not cure the deficiencies of *Shin*, *Locker*, or both.

Further, even if the references were combined as suggested by the Examiner, the combination of the cited references fails to disclose or suggest circuitry that operates responsive to the hint signal to generate data transfer control signals for controlling the third circuit portion in order to control output of the data blocks.

For at least the foregoing reasons, the combination of the *Shin*, *Locker* and *Arimilli* references fails to teach or suggest all the limitations the pending base claims. Accordingly,

Applicant respectfully submits that base claims are therefore in condition for allowance over the applied art of record. Claims 3-7 depend from base claim 1 and introduce additional limitations therein. Likewise, claim 14 depends from base claim 13 and introduces additional limitations therein. Accordingly, these dependent claims are also believed to be in condition for allowance.

With regard to claims 2, 8, 9, 11, 12, 15, and 16, which are rejected over *Shin*, *Locker* and *Arimilli* in combination with *Naumann*, Applicant submits that the *Naumann* reference does not cure the deficiencies of the *Shin* reference. *Naumann* does not use hint signals and, at a minimum, does not meet the limitations of generating, in response to the header block, a hint signal that gives advance notification of a data transfer operation, the hint signal being operable to be transferred via a synchronizer.

Based on the foregoing, Applicant respectfully submits that claims 2, 8, 9, 11, 12, 15, and 16 are also in condition for allowance over the applied art of record.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and/or amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: 5/6/08

Shreen K. Danamraj
Registration No. 41,696

Correspondence Address

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Please direct telephone calls to:

Steven L. Webb
(970) 898-3471